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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,253	06/17/2005	Andreas Przadka	14219-075US1/P2002,0539 U	8747

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EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/521,253	PRZADKA, ANDREAS	
	Examiner	Art Unit	
	Eduardo A. Rodela	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/17/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: The disclosure states that the multi-layer substrate comprises layers of Silicone or Silicone Oxide, which is never used in the art as an insulator on a multi-layered wiring board and needs to be changed to Silicon or Silicon Dioxide ("SiO2" or "Si" or "Silicon Oxide (SiO2)"). Appropriate correction is required.

Claim Objections

Claim 17 objected to because of the following informalities: The claim states that the multi-layer substrate comprises layers of Silicone or Silicone Oxide, which is never used in the art as an insulator on a multi-layered wiring board and needs to be changed to Silicon or Silicon Dioxide ("SiO2" or "Si" or "Silicon Oxide (SiO2)"). Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 10-23, 25-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Ogino et al. (US 6,889,155).

Regarding claim 1, Ogino et al. discloses an electronic component comprising a multi-layer substrate having an upper side and under side [Fig. 7: multi-layer substrate, including base board 2 and high frequency circuit 3], the multi-layer substrate comprising at least one integrated impedance converter [column 9: lines 15-22]; and at least one chip component comprising external contacts [Fig. 7: semiconductor chip 26], the at least one chip component being disposed on the upper side of the multi-layer substrate, the at least on chip component being electrically connected to the at least one integrated impedance converter [Fig. 7: surface mounted by solder balls 27].

Regarding claim 2, Ogino et al. discloses the electronic component of claim 1, wherein the external contacts comprise surface mounted device contacts [Fig. 7: surface mounted by solder balls 27].

Regarding claim 3, Ogino et al. discloses the electronic component of claim 1 wherein the multi-layer substrate comprises, at least one passive circuit element or at least one active circuit element [Fig. 6: passive element 136].

Regarding claim 4, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip component comprising at least one filter circuit [column 1: line 50 through column 2: line 11].

Regarding claim 5, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip component comprises at least one resonator that operates with surface acoustic waves [column 1: line 50 through column 2: line 11].

Regarding claim 7, Ogino et al. discloses the electronic component of claim 1 wherein the at least one chip component comprises a microwave ceramic filter [Since

the microwave frequency range is roughly defined as 1GHz-500Ghz, Ogino's electronic component operates between this range as disclosed in column 1: lines 23-32, and the component is shown to have integral capacitors disclosed in Fig. 7: 19 and 20, and the device is made of ceramic insulator as disclosed in column 9: lines 23-35].

Regarding claim 10, Ogino et al. discloses the electronic component of claim 1, wherein the at least one discrete circuit element disposed on the upper side of the multi-layer substrate, the at least on discrete circuit element comprising an active circuit element or a passive circuit element [column 1: line 50 through column 2: line 11].

Regarding claim 11, Ogino et al. discloses the electronic component of claim 10, wherein the at least one discrete circuit element comprises at least one of the following: a high-frequency circuit, an adjustment circuit, an impedance converter, etc. [column 1: line 50 through column 2: line 11].

Regarding claim 12, Ogino et al. discloses the electronic component of claim 10, wherein the at least one discrete circuit element comprises at least part of a high-frequency circuit, a duplexer or a diplexer, and wherein the at least on discrete circuit element assists in connecting the at least one chip component to an antenna [column 1: line 50 through column 2: line 11].

Regarding claim 13, Ogino et al. discloses the electronic component of claim 1, further comprising: at least one circuit element integrated in the multi-layer substrate; wherein the at least one circuit element comprises at least part of one of the following: a high frequency circuit, an adjustment circuit, etc. [column 1: line 50 through column 2: line 11, and Fig. 7: integral devices 11 and 18-22].

Regarding claim 14, Ogino et al. discloses the electronic component of claim 13, wherein the at least part of an adjustment circuit integrated in the multi-layer substrate is formed as one or more strip conductors on the upper side of the multi-layer substrate [column 1: line 50 through column 2: line 11, and Fig. 7: integral devices 18-22 which are formed as deposited metallic conductive strip].

Regarding claim 15, Ogino et al. discloses the electronic component of claim 1, wherein the multi-layer substrate comprises a plurality of adjustment circuits [column 1: line 50 through column 2: line 11, and Fig. 7: integral devices 18-22].

Regarding claim 16, Ogino et al. discloses the electronic component of claim 1, wherein the multi-layer substrate comprises ceramic layers [column 9: line 23-35].

Regarding claim 17, Ogino et al. discloses the electronic component of claim 1, wherein the multi-layer substrate comprises layers of Silicon and Silicon "Oxide" (Silicon Dioxide or SiO2) [column 2: line 66 to column 3: line 6, and column 10: line 3-11].

Regarding claim 18, Ogino et al. discloses the electronic component of claim 1, wherein the multi-layer substrate comprises one or more layers of an organic material [column 9: lines 23-35].

Regarding claim 19, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip comprises at least one or more inputs and outputs; and wherein at least one input and/or at least one output of the at least one chip component conducts an asymmetrical signal [Fig. 7: semiconductor chip 26 and Fig. 6: discrete device 136, both inherently have at least one input and at least one output, and the discrete device, will handle asymmetrical or "analog" signals].

Regarding claim 20, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip component comprises at least one or more inputs and outputs; and wherein at least one input and/or at least one output of the at least one chip component conducts a symmetrical signal [Fig. 7: semiconductor chip 26 and Fig. 6: discrete device 136, both inherently have at least one input and at least one output, and the semiconductor chip, will handle symmetrical or "digital" signals].

Regarding claim 21, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip component comprises a connection to ground, the connection to ground being made via an adjustment circuit that is at least partially integrally integrated in the multi-layer substrate; and wherein the adjustment circuit comprises at least one of a coil, a capacitor, and a conductor [Fig. 7: semiconductor chip 26 connects through resistor 22 and integral functional filters 11 to ground pattern 14, column 8: lines 1-53].

Regarding claim 22, Ogino et al. discloses the electronic component of claim 10, wherein the at least one chip component and the at least one discrete circuit element comprise surface mounted design elements [Fig. 7: semiconductor chip 26 and Fig. 6: discrete device 136, column 9: lines 45-56].

Regarding claim 23, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip component comprises a housing comprising external contacts [Fig. 6: housing 150, 152, 157 comprising external contacts 154].

Regarding claim 25, Ogino et al. discloses the electronic component of claim 1, wherein the at least one chip component is connected to the multi-layer substrate via flip-chip technology [column 9: lines 45-56].

Regarding claim 26, Ogino et al. discloses a method of producing an electronic component comprised of a multi-layer substrate having an upper side and under side [Fig. 7: board with parts 2 and 3], the multi-layer substrate comprising at least one integrated impedance converter [Fig. 7: integral components 11, 19-22 which provide signal integrity as disclosed in column 2: lines 1-11, column 8: lines 29-54], and at least one chip component comprising external contacts [Fig. 7: chip 26 has contacts connected to by solder balls 27], the method comprising installing the at least one chip component in a housing [it is inherent that a chip component would be in a housing, which is done to isolate the device from impurities which would degrade its performance]; and mounting the housing onto the upper side of the multi-layer substrate so as to electrically connect the at least one chip component to the integrated impedance converter [Fig. 7: chip 26 connects to wiring board with parts 2 and 3 through solder balls 27 to integral components of the device 11, 18-22, which have the purpose disclosed in column 2: lines 1-11].

Regarding claim 27, Ogino et al. discloses the method of claim 26 further comprising: mounting at least one discrete circuit element on the upper side of the multi-layer substrate [Fig. 6: discrete element 136].

Regarding claim 28, Ogino et al. discloses the method of claim 27, wherein the at least one chip component and the at least one discrete circuit element are attached to

the upper side of the multi-layer substrate using a same attaching mechanism [soldering connections used to connect the two devices, Fig. 6: discrete element 136 and chip 136 are connected by solder connection].

Regarding claim 29, Ogino et al. discloses the method of claim 27, wherein the at least one chip component and/or the at least one discrete circuit element is mechanically stabilized using a casing compound [Fig. 6: discrete element 136 and chip 136 are encapsulated by shield cover 157].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogino et al. (US 6,889,155).

Regarding claim 6, Ogino et al. discloses the electronic component of claim 1. Ogino et al. does not specifically disclose the at least one chip component comprises a resonator that operates with bulk acoustic waves. Ogino et al. does disclose a reference frequency generating circuit, which would include an oscillating crystal, which could be a Bulk Acoustic Wave device [column 1: line 50 through column 2: line 11]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a Bulk Acoustic Wave device in a reference frequency generating circuit. The ordinary artisan would have been motivated to use the Bulk Acoustic Wave device

to provide a necessary clock signal and reduce the electronic components' overall signal dependency.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogino et al. (US 6,889,155) in view of Asahi et al. (US 6,955,948).

Regarding claim 8, Ogino et al. discloses the electronic component of claim 1, and that it contains inductors, capacitors, and resistors to be used in characteristic analog circuits, normally used in high frequency receiving and transmitting circuits. Ogino et al. does not specifically disclose a LC chip filter. Asahi et al. discloses the at least one chip component comprises an inductive-capacitive (LC) chip filter [column 9: lines 10-17]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a LC filter in a high frequency circuit used in receiving and transmitting circuits. The ordinary artisan would have been motivated to use the LC filter to provide the necessary filtering, modulation, and various other signal shaping functions necessary to the task.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogino et al. (US 6,889,155) in view of Figueroa et al. (US 6,338,207).

Regarding claim 9, Ogino et al. discloses the electronic component of claim 1, and the use of several filters [Ogino, column 1: line 50 through column 2: line 11]. Ogino et al. does disclose the at least one chip component comprises a stripline filter. Figueroa et al. discloses the at least one chip component comprises a stripline filter [capacitor used as signal filter to deliver improved signal integrity through the substrate to the semiconductor chips, disclosed in column 3: lines 24-34, column 4: lines 1-10,

and column 6: lines 24-34]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a stripline filter. The ordinary artisan would have been motivated to such a device to improve the signal quality being fed through the substrate to the supported electronic component.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogino et al. (US 6,889,155) in view of Okabe et al. (US 6,757,178).

Regarding claim 24, Ogino et al. discloses the electronic component of claim 1. Ogino et al. does not disclose the at least one chip component is connected to the multi-layer substrate via wire bonding. Okabe et al. does disclose the at least one chip component is connected to the multi-layer substrate via wire bonding [Fig. 1: 40 connects to multi-layer board by wire bonding 41a and 41b]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use wire bonding for electrical connection. The ordinary artisan would have been motivated to make such a connection due to the standard and trusted nature of the method of electrical connection and also as an alternative to the contact-to-contact solder reflow process.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571) 272-8797. The examiner can normally be reached on M-F, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 5712721915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eduardo A. Rodela
Examiner

Zandra V. Smith
Primary Examiner

Eduardo A. Rodela